

APPARATUS FOR REDUCING A MAGNITUDE OF A RATE OF CURRENT CHANGE OF AN INTEGRATED CIRCUIT

Abstract

An apparatus for reducing a magnitude of a rate of current change of an integrated circuit is provided. The method uses a counter stage controlled by a control stage to sequentially disable a plurality of transistors that are used to source current from a power supply. By sequentially disabling the plurality of transistors, a reduction of an amount of current occurs gradually, effectively reducing the magnitude of the rate of current change.

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